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(54) [Title of Invention] STACKED CAPACITOR ARRAY PROVIDED WITH VARISTOR FUNCTION

(57) [Abstract]

[Object] The object of the present invention is to absorb a high-frequency noise and surge and to prevent effectively a cross-talk between several signal lines even when the inner conductors connected to several signal lines are formed with a higher density.

[Structure] A laminate 65 consists of dielectric sheets 10, 20, 30 having a capacity and a varistor characteristic. In the sheet 10, inner conductors 11a, 11b connected to one side of the sheet and having spacers electrically insulating them from the remaining three sides of the sheet are provided on the sheet surface. In the sheet 30, an inner conductor 31 is provided on the sheet surface in the same manner as in sheet 10. In the sheet 20 serving as an intermediate sheet, a ground conductor 23 is provided on the sheet surface, this ground electrode being insulated from a pair of sides corresponding to those sides of sheets 10 and 30 which are connected to the inner conductors and being connected to the other pair of sides. The capacitance is formed between the inner conductor and ground conductor via sheets 20, 30. Signal electrodes 51, 52 connected to the inner conductors and a pair of ground electrodes 53, 54 connected to the ground conductor are formed independently on the side surfaces of the laminate.

[Patent Claims]

[Claim 1] A stacked capacitor array provided with a varistor function comprising a laminate (65, 115) obtained by laminating and integrating a first dielectric sheet (10, 60) having a capacity and a varistor characteristic and a third dielectric sheet (30, 80) having a capacity and a varistor characteristic via a rectangular second dielectric sheet (20, 70) having a capacity and a varistor characteristic as an intermediate sheet, wherein the first dielectric sheet has the same shape and size as the second dielectric sheet (20, 70) and the second dielectric sheet has the same shape and size as the second dielectric sheet (20, 70),

in said first dielectric sheet (10, 60), first inner conductors (11a, 11b, 61) electrically connected to one side and having spacers (14, 62, 63, 64) electrically insulating them from the remaining three sides are provided on the sheet surface,

in said third dielectric sheet (30, 80), a second inner conductor (31, 81) is provided on the sheet surface, this second inner conductor being electrically connected to one side opposite to one side of the first dielectric sheet (10, 60) which is electrically connected to said first inner conductor (11a, 11b, 61) and having spacers (32, 82, 83, 84) electrically insulating it from the remaining three sides,

in said second dielectric sheet (20, 70), a ground conductor (23, 73) is provided on the sheet surface, this ground conductor having spacers (21, 22, 71, 72) electrically insulating it from a pair of sides corresponding to those sides of the first and third dielectric sheets (10, 30, 60, 80) which are electrically connected to said first and second inner conductors (11a, 11b, 31, 61, 81) and being electrically connected to a pair of sides other than said pair of sides,

the structure being such that a respective capacitance is formed between said first inner conductors (11a, 11b, 61) and said ground conductor (23, 73) via said second dielectric sheet (20, 70), and between said second inner conductor (31, 81) and said ground conductor (23, 73) via said third dielectric sheet (30, 80),

first and second signal electrodes (51, 51, 52, 101, 102) respectively connected to said first and second inner conductors (11a, 11b, 31, 61, 81) exposed on the side surface of said laminate (65, 115) are formed on its side surface,

a pair of first and second ground electrodes (53, 54, 103, 104) connected to said ground conductors (23, 73) exposed on other two side surfaces of said laminate (65, 115) are formed on these two side surfaces.

[Claim 2] A stacked capacitor array provided with a varistor function as described in Claim 1, wherein a fourth dielectric sheet (40, 90) which has no conductor formed on the sheet surface is laminated and integrated as an outermost layer in the laminate (65, 115).

[Detailed Description of the Invention]

[0001]

[Field of Industrial Utilization] The present invention relates to a stacked capacitor array provided with a varistor function which absorbs high-frequency noise and surge voltage in a several signal lines. More specifically, the present invention relates to a stacked capacitor array

provided with a varistor function, which is suitable for preventing cross-talk between several signal lines.

[0002]

[Prior Art Technology] In digital devices such as computers, the penetration of a high-frequency noise or abnormal voltage (surge) can easily cause malfunction. Another problem associated with such devices is that lines can emit unnecessary electromagnetic waves which can damage other electronic devices. For this reason, surface absorbers removing a surge voltage and noise filters removing a high-frequency noise have been used in signal lines. Varistors, Zener diodes, discharge elements and the like have been used for the surge absorbers, and capacitor elements have been used for the noise filters. Those electronic components such as surface absorbers and noise filters have been installed in each signal line, and surge countermeasures and noise countermeasures were implemented separately from each other, as shown by the circuit diagrams shown in Fig 10. However, when these countermeasures are implemented by separate electronic components, the space taken by the components is increased and the cost is raised.

[0003] In order to resolve the above-described problems, "a filter absorbing high frequency and surges" was suggested (Unexamined Japanese Patent Application 1-102874). The filter comprised a thin narrow signal line for electric signal transmission, which was formed on one surface of a flat plate made of a dielectric material having a capacity and a varistor characteristic. A ground electrode was formed on almost the whole other surface of the plate, and a varistor and a distributed-constant capacitor were formed between the signal line and the ground electrode. Such a filter could absorb a high-frequency noise and surge voltage.

[0004]

[Problems Addressed by the Invention] When a high-frequency noise and surge voltage present in several signal lines were absorbed by using the filter disclosed Unexamined Japanese Patent Application 1-102874, if the space between several signal lines arranged in a row on one surface of the plate was small and a high-frequency signal was passed through a signal line, because of a floating capacitance present between the wires, a noise having a frequency above a certain value was transmitted to other signal lines and cross-talk could easily occur. For this reason, it was difficult to arrange a plurality of signal lines with a high density in the above-described filter.

[0005] It is an object of the present invention to provide a stacked capacitor array with a varistor function which can remove a high-frequency noise, absorb a surge, and prevent reliably a cross-talk between a signal passing through a signal line and another line even when the inner conductors connected to several signal lines are formed with a density higher than that in the conventional arrays.

[0006]

[Means to Resolve the Problems] A structure of the present invention developed to attain the above-described object will be described below with reference to Fig 1 – Fig 4. In order to facilitate the explanation, the ceramic sheets in Figs 1, 2, and 4 are expanded in the thickness

direction. The stacked capacitor array provided with a varistor function in accordance with the present invention comprises a laminate 65 obtained by laminating and integrating a first dielectric sheet 10 having a capacity and a varistor characteristic and a third dielectric sheet 30 having a capacity and a varistor characteristic via a rectangular second dielectric sheet 20 having a capacity and a varistor characteristic as an intermediate sheet, wherein the first dielectric sheet has the same shape and size as the second dielectric sheet 20 and the second dielectric sheet has the same shape and size as the second dielectric sheet 20. In the first dielectric sheet 10, first inner conductors 11a, 11b electrically connected to one side of the sheet and having a spacer 14 electrically insulating it from the remaining three sides is provided on the sheet surface. In the third dielectric sheet 30, a second inner conductor 31 is provided on the sheet surface, this second inner conductor being electrically connected to one side opposite to one side of the first dielectric sheet 10, which is electrically connected to the first inner conductors 11a, 11b, and having a spacer 32 electrically insulating it from the remaining three sides. In the second dielectric sheet 20, a ground conductor 23 is provided on the sheet surface, this ground conductor having spacers 21, 22 electrically insulating it from a pair of sides corresponding to those sides of the first and third dielectric sheets 10, 30, which are electrically connected to the first and second inner conductors 11a, 11b, and being electrically connected to a pair of sides other than said pair of sides. The structure of the array is such that a respective capacitance is formed between the first inner conductors 11a, 11b and the ground conductor 23 via the second dielectric sheet 20, and between the second inner conductor 31 and the ground conductor 23 via the third dielectric sheet 30. The first and second signal electrodes 51, 51, 52 respectively connected to the first and second inner conductors 11a, 11b, 31 exposed on the side surface of the laminate 65 are formed on its side surface. A pair of first and second ground electrodes 53, 54 connected to the ground conductors 23 exposed on other two side surfaces of the laminate 65 are formed on these two side surfaces. In this specification, the expression "dielectric sheet having a capacity and a varistor characteristic" refers to a sheet which demonstrates a surface absorption function due to a varistor characteristic and also a has a dielectric characteristic in a voltage range below the varistor voltage.

[0007]

[Operation] Since the ground conductor 23 is connected via ground electrodes 53, 54 between the first inner conductors 11a, 11b on the first dielectric sheet 10 and second inner conductor 31 on the third dielectric sheet 30, the floating capacitance between the neighboring signal lines is substantially eliminated and the signal or noise cross-talk between the lines is prevented. Furthermore, since a capacitance is formed between the first inner conductors 11a, 11b and the ground conductor 23 via the second dielectric sheet 20, and between the second inner conductor 31 and the ground conductor 23 via the third dielectric sheet 30, a difference in potential appears between the ground conductor 23 and inner conductors 11a, 11b, 31 which are in a conductive state, the system functions as a capacitor in a voltage range below the varistor voltage, and the high-frequency noise is absorbed. Furthermore, if a surge voltage is applied to the signal lines, the respective differences in potential exceeding the varistor voltage are generated between the ground conductor 23 and inner conductor 31, dielectric sheet 10 between the inner conductors 11a, 11b, and dielectric sheet 20 between the inner conductors 11a, 11b and ground conductor 23. As a result, owing to a varistor characteristic of the dielectric sheets 10, 20, the surge current is passed through the respective ground conductors 23 and removed via the ground electrodes 53,

54. Furthermore, since the ground conductor 23 is provided between the inner conductor connected to a signal line to which a surge voltage was applied and other inner conductor and only a difference in potential which is generated by the normal signal appears between the inner conductors, the effect of the transmitted surge is limited only to the inner conductor to which the surge voltage was applied.

[0008]

[Embodiments] The embodiments of the present invention will be described below. The present invention is not limited to these embodiments.

<Embodiment 1> A stacked capacitor array of Embodiment 1 will be described below with reference to Fig 1 to Fig 5. First, four ceramic green sheets of the same shape and size were prepared from a dielectric material having an electric capacity varistor characteristic, for example, semiconductor varistor material based on zinc oxide, strontium titanate, titanium oxide or the like. Those sheets were referred to as a first sintered ceramic sheet, second sintered ceramic sheet, third sintered ceramic sheet, and fourth sintered ceramic sheet, respectively.

[0009] Then, an electrically conductive paste containing Pd as the main component was screen printed on the front surface of the first sintered ceramic sheet, second sintered ceramic sheet, and third sintered ceramic sheet so as to form respective different patterns, and the printed paste was dried for 4 min at a temperature of 80°C. Thus, as shown in Fig 3, first inner conductors 11a, 11b were formed by printing on the surface of the first sintered ceramic sheet 10. Those inner conductors were electrically connected to one side of the sheet and had spacers 14 which electrically insulated them from the three other sides of the sheet. Further, a ground conductor 23 was formed by printing on the surface of the second sintered ceramic sheet 20. This ground conductor had spacers 21, 22 which electrically insulated it from two opposite sides of the sheet, was electrically connected to two opposite sides other than the above-mentioned opposite sides, and had a portion overlapping the inner conductors 11a, 11b formed on the first sintered ceramic sheet 10 upon stacking. Moreover, a second inner conductor 31 was formed by printing on the surface of the third sintered ceramic sheet 30. The second inner conductor had a portion overlapping the ground conductor 23 formed on the second sintered ceramic sheet upon stacking, was electrically connected to one side of the sheet which was opposite to the above-mentioned one side of the first sintered ceramic sheet which was electrically connected to the first inner conductors 11a, 11b, and had a spacer 32 that electrically insulated it from other three sides of the sheet.

[0010] The screen-printed three sheets (first, second, and third sintered ceramic sheets 10, 20, 30) were stacked in the order of description and then a fourth sintered ceramic sheet 40 that was not printed with the electrically conductive paste was laminated as an uppermost layer. Those green sheets represent respective dielectric sheets in accordance with the present invention. The laminate 65 shown in Fig 4 was integrated by thermal pressing and then fired for about 1 h at a temperature of 1300°C to give a sintered body having a thickness of about 1 mm. As shown in Fig 4, the sintered body was barrel polished to expose the first inner conductors 11a, 11b, second inner conductor 31 (not shown in Fig 4), and ground conductor 23 on the side surface of the sintered body.

[0011] Then, as shown in Fig 5, an electrically conductive paste containing Ag as the main component was coated on the portion of the side surface of the sintered body where the inner conductors 11a, 11b, 31 and ground conductor 23 were exposed. The coated paste was fired to form signal electrodes 51, 51, 52 and ground electrodes 53, 54. As a result, a stacked capacitor array was obtained in which the first inner conductors 11a, 11b were electrically connected to the first signal electrode 51, the second inner conductor 31 was electrically connected to the second signal electrode 52, and the ground conductor 23 was electrically connected to the first and second ground electrodes 53, 54.

[0012] In order to study characteristics of the stacked capacitor array, it was mounted on a printed substrate 55 that was separately prepared for the test. In the printed substrate 55, three signal lines 56a, 56b, and 57 were printed on the upper surface of the substrate, and ground electrodes 58 and 59 were formed on both sides of these lines. The respective through holes 58a and 59a were provided in the electrodes 59, 59, and the electrodes 58 and 59 were electrically connected to the ground electrode 55a formed over almost the whole lower surface of the substrate 55 via the through holes 58a and 59a. The ground electrode 55a was grounded. Signal electrodes 51, 51 were soldered to respective signal lined 56a, 56b, the signal electrode 52 was soldered to the signal line 57, and ground electrodes 53, 54 were soldered to respective ground electrodes 58, 59.

[0013] In this state, a high-frequency signal was input from one end of signal lines 56a, 56b and 57, the output signal was measured at the other end, and the insertion loss was determined. The results obtained demonstrated that the insertion loss rapidly increased with the increase in frequency, and the stacked capacitor array had a good filter characteristic. Then, the existence of cross-talk was studied by measuring the output signals at the other ends of the neighboring signal lines 56a and 57 or other ends of signal lines 56b and 57. The results obtained confirmed that the cross-talk was so small that could not be detected, which was a significant improvement over the results obtained by conducting measurements on the conventional high-frequency and surge-absorbing filter. Then, a surface voltage exceeding a varistor voltage of the dielectric sheets 10, 20, and 30 was applied to one end of signal lines 56a, 56b, and 57, and a voltage between the other end of the signal line and the adjacent signal line was measured. The results obtained demonstrated that a voltage equivalent to surge limit voltage on a varistor characteristic was absorbed at the other end of the signal line to which a voltage has been applied, and a surge-absorbing function was confirmed. A normal voltage that was unaffected by the surface voltage was detected at the neighboring signal lines.

[0014] <Embodiment 2> A stacked capacitor array of Embodiment 2 will be described below with reference to Fig 6 – Fig 9. In Fig 6 – Fig 9, symbols assigned to various structural components corresponding to those in Embodiment 1 are obtained by adding 50 to the symbols employed in Embodiment 1. First, four ceramic green sheets of the same shape and size were prepared in the same manner as in Embodiment 1. Those sheets were referred to as a first sintered ceramic sheet, second sintered ceramic sheet, third sintered ceramic sheet, and fourth sintered ceramic sheet, respectively.

[0015] Then, an electrically conductive paste containing Pd as the main component was screen printed on the front surface of the first sintered ceramic sheet, second sintered ceramic sheet, and third sintered ceramic sheet so as to form the respective different patterns, and the printed paste was dried for 4 min at a temperature of 80°C. Thus, as shown in Fig 7, a first inner conductor 61 was formed by printing on the surface of the first sintered ceramic sheet 60. This inner conductor was electrically connected to one side of the sheet and had spacers 62, 63, and 64 which electrically insulated them from the three other sides of the sheet. Further, a ground conductor 73 was formed by printing on the surface of the second sintered ceramic sheet 70. This ground conductor had spacers 62, 63 which electrically insulated it from two opposite sides of the sheet and spacers 71, 72 which electrically insulated it from two opposite sides of the sheet other than the above-mentioned pair of opposite sides, and had a portion overlapping the inner conductor 61 formed on the first sintered ceramic sheet 60 upon stacking. Moreover, a second inner conductor 81 was formed by printing on the surface of the third sintered ceramic sheet 80. The second inner conductor had a portion overlapping the ground conductor 73 formed on the second sintered ceramic sheet 70, was electrically connected to one side of the sheet which was opposite to the above-mentioned one side of the first sintered ceramic sheet 60 which was electrically connected to the first inner conductor 61, and had spacers 82, 83, and 84 that electrically insulated it from other three sides of the sheet.

[0016] The screen-printed three sheets (first, second, and third sintered ceramic sheets 60, 70, 80) were stacked in the order of description and then a fourth sintered ceramic sheet 90 that was not printed with the electrically conductive paste was laminated as an uppermost layer. The laminate was integrated by thermal pressing. The laminate 115 shown in Fig 8 was fired similarly to Embodiment 1 to give a sintered body which was barrel polished to expose the first inner conductor 61, second inner conductor 81 (not shown in Fig 8), and ground conductor 73 on the side surface of the sintered body.

[0017] Then, as shown in Fig 9, an electrically conductive paste containing Ag as the main component was coated on the portion of the side surface of the sintered body where the inner conductors 61, 81 and ground conductor 73 were exposed. The coated paste was fired to form signal electrodes 101, 102 and ground electrodes 103, 104. As a result, a stacked capacitor array was obtained in which the first inner conductor 61 and second inner conductor 81 were electrically connected to the first and second signal electrodes 101, 102, and the ground conductor 73 was electrically connected to the first and second ground electrodes 103, 104.

[0018] The stacked capacitor array was mounted on a printed substrate that was separately prepared for the test, and the characteristics were studied in the same manner as in Embodiment 1. A high-frequency signal was input from one end of signal lines (not shown in the figures) connected to signal electrodes 101, 102, the output signal was measured at the other end, and the insertion loss was determined. The results obtained demonstrated that the insertion loss rapidly increased with the increase in frequency, and the stacked capacitor array had a good filter characteristic. Then, the existence of cross-talk was studied by measuring the output signals at the other ends of signal lines (not shown in the figures) connected to signal electrodes 101, 102. The results obtained confirmed that the cross-talk was so small that could not be detected, which was a significant improvement over the results obtained by conducting measurements on the conventional high-frequency and surge-absorbing filter. Then, a surface voltage exceeding a

varistor voltage of the dielectric sheets 60, 70, and 80 was applied to one end of signal lines (not shown in the figures) connected to signal electrodes 101, 102, and a voltage between the other ends of the signal lines and the adjacent signal lines was measured. The results obtained demonstrated that a voltage equivalent to a surge limit voltage on a varistor characteristic is absorbed at the other end of the signal line to which a voltage has been applied, and a surge-absorbing function was confirmed. A normal voltage that was unaffected by the surface voltage was detected at the neighboring signal lines.

[0019] In Embodiment 1 and Embodiment 2, a laminate was obtained by laminating one first, one second, and one third ceramic green sheet. However, in accordance with the present invention, no limitation is placed on the number of first ceramic green sheets, second ceramic green sheets, and third ceramic green sheets. Thus, by appropriately increasing the number of those sheets in the laminate, it is possible to change the capacitance formed by the inner conductors and ground conductors, to change the insertion loss, and at the same time to increase surge resistance. Furthermore, in Embodiment 1, two first inner conductors and one second inner conductor were used. However, the present invention is not limited to those numbers of the first inner conductors and second inner conductors, and those numbers can be increased. When a plurality of inner conductors of each type are used, the arrangement in which the inner conductors on a separate sheet are positioned between the neighboring inner conductors is preferred from the standpoint of preventing the cross-talk. Furthermore, when a separate protective means is installed on the third dielectric sheet, it is possible to produce a laminate without the fourth dielectric sheet which served as an uppermost layer.

[0020]

[Effect of the Invention] As described above, in accordance with the present invention, at least two signal electrodes are electrically connected to signal lines or signal leads employed for signal transmission. As a result, a capacitance is formed between the first inner conductor of the first dielectric sheet and the ground conductor of the second dielectric sheet, and between the second inner conductor of the third dielectric sheet and the ground conductor of the second dielectric sheet. Therefore, a high-frequency noise penetrating into the signal line or the like can be prevented. Furthermore, when a surge voltage is applied to the signal electrodes, a difference in potential exceeding the varistor voltage is generated in the second dielectric sheet and third dielectric sheet between the inner conductors and ground conductors, the surge current passes through the ground conductors and is removed via the ground electrode. When the surge is absorbed, the surge produces no adverse effect on the inner conductors other than the inner conductor to which the surge voltage was applied, owing to the presence of the ground electrodes. Furthermore, since a ground conductor is arranged between the first inner conductor and second inner conductor, and this ground conductor is grounded via the ground electrode, the floating capacitance can be removed with higher reliability even if a high-frequency signal is supplied to the signal line, and the cross-talk between the neighboring signal lines can be prevented. As a result, a stacked capacitor array provided with a varistor function can be obtained, which has small dimensions and both the high-frequency noise removal function and surge absorption function, and in which the cross-talk between the signal in any signal line and other line can be effectively prevented even when the inner conductors connected to a plurality of signal lines are arranged with a high density.

[Brief Description of the Drawings]

Fig 1 is a cross section along the A-A line in Fig 5 illustrating the stacked capacitor array which is an embodiment of the present invention.

Fig 2 is a cross section along the B-B line relating to the same embodiment.

Fig 3 is a perspective view of the laminate prior to firing.

Fig 4 is a perspective view of a sintered body obtained by firing the laminate.

Fig 5 is a perspective view of a stacked capacitor array mounted onto a printed substrate.

Fig 6 is a cross section along the C-C line in Fig 9 illustrating the stacked capacitor array which is another embodiment of the present invention.

Fig 7 is a perspective view of the laminate prior to firing.

Fig 8 is a perspective view of a sintered body obtained by firing the laminate.

Fig 9 is a perspective view of the stacked capacitor array.

Fig 10 shows equivalent circuits of the conventional noise filter and surge absorber.

[Legends]

10, 60 : first dielectric sheet (first ceramic green sheet)
11a, 11b, 61 : first inner conductor
14, 64 : electrically insulating spacers
20, 70 : second dielectric sheet (second ceramic green sheet)
21, 22, 71, 72 : electrically insulating spacers
23, 73 : ground conductors
30, 80 : third dielectric sheet (third ceramic green sheet)
31, 81 : second inner conductor
32, 82, 83, 84 : electrically insulating spacers
40, 90 : fourth dielectric sheet (fourth ceramic green sheet)
51, 101 : first signal electrode
52, 102 : second signal electrode
53, 103 : first ground electrode
54, 104 : second ground electrode
65, 115 : laminate

Fig 1

10 : first dielectric sheet (first ceramic green sheet)
11a, 11b : first inner conductor
14 : electrically insulating spacers
20 : second dielectric sheet (second ceramic green sheet)
23 : ground conductors
30 : third dielectric sheet (third ceramic green sheet)
31 : second inner conductor
32 : electrically insulating spacers
40 : fourth dielectric sheet (fourth ceramic green sheet)
53 : first ground electrode

54 : second ground electrode

Fig 2

Fig 3

Fig 4
65 : laminate

Fig 5

Fig 6

60 : first dielectric sheet (first ceramic green sheet)
61 : first inner conductor
64 : electrically insulating spacers
70 : second dielectric sheet (second ceramic green sheet)
73 : ground conductors
80 : third dielectric sheet (third ceramic green sheet)
81 : second inner conductor
84 : electrically insulating spacers
90 : fourth dielectric sheet (fourth ceramic green sheet)
101 : first signal electrode
102 : second signal electrode

Fig 7

Fig 8
115 : laminate

Fig 9

Fig 10